

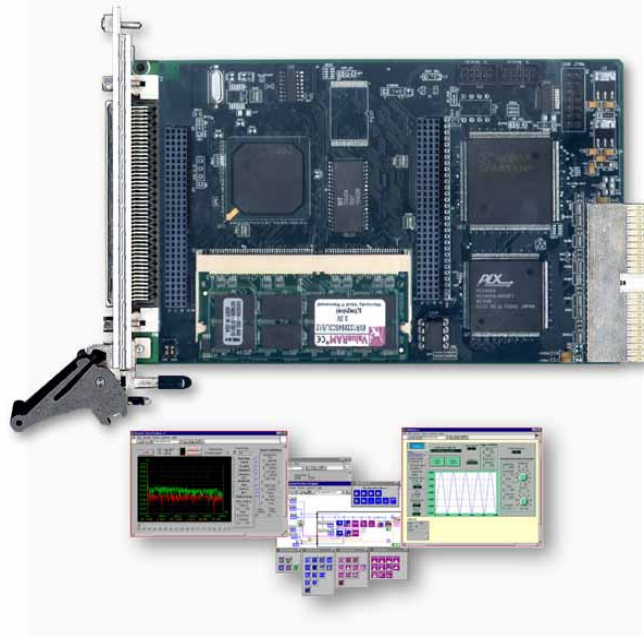


SI-C671xDSP-cPCI

C671x DSP Board for CompactPCI/PXI Bus

Key Features

- 1800 MFLOPS peak performance with C6713, 32 bit floating/fixed point precision.
- Up to 256MB SDRAM, using conventional PC133 SDRAM SO-DIMM format.
- Full 32 bit bi-directional PCI initiated bus mastering, with 132MB/sec peak transfer rate.
- Memory mapped host communications port.
- Software development tools from Sheldon Instruments includes [QuVIEW](#), [QuBASE](#) and the [SI-DDKs](#); as well compatibility with separately purchased TI and third party tools.
- Windows and Linux 32/64 bit drivers and sample application support.
- Expansion connectors for prototyping, analog & digital I/O daughter cards.
- Small 3U form factor.
- JTAG port for in system development and debugging.



Introduction

The SI-C6xDSP-cPCI from Sheldon Instruments is a powerful Digital Signal Processor (DSP) card for your system equipped with a cPCI/PXI bus. It is based on Texas Instruments' 225-300Mhz TMS320C6713, 32 bit DSP, and can transform your cPCI/PXI chassis into an ultra high performance development system and DSP accelerator. A full line of software development tools are available from Sheldon Instruments and TI, which include compilers, assemblers, linkers, and debuggers.

Host cPCI/PXI bus to DSP Link

The hardware interface between the host cPCI/PXI bus and the DSP is implemented with PLX's PCI9054 device. Onboard control logic arbitrates the appropriate timing between the C6x's EMIF bus, the boot SRAM/Flash, and the PCI9054's local bus. A combination of hardware and software handshaking takes place in order to support a myriad of data transfer schemes, where the host side can be selected to operate in one mode and the DSP in another. From the host cPCI/PXI side, three (3) modes are available: 1) target/slave mode, 2) PCI initiated bus mastered transfer mode with the PCI9054 acting as the bus master, and 3) bus mastering with the DSP acting as the PCI bus master. From the DSP side,



three (3) modes are available: 1) standard programmed I/O, 2) asynchronous DMA, and 3) synchronous DMA.

Host target/slave mode accesses are performed when the DSP is either disabled (reset asserted) or enabled (reset deasserted). While the DSP is disabled, the host uses target/slave mode transfers to load an initialization COFF file to the card's boot SRAM/Flash memory, as well as to access expansion daughter modules. After DSP activation, any combination of data transfer modes can be used on either side.

For most applications, the most efficient method of large data block transfer is to use cPCI/PXI bus mastering, as it requires minimal host intervention. The first bus master method involves using the PCI9054's DMA engine, in conjunction with the DSP using programmed I/O or its own DMA engine. The second bus master transfer method allows the DSP to act as the PCI bus master, where it actually has direct access to the host computer's main memory!

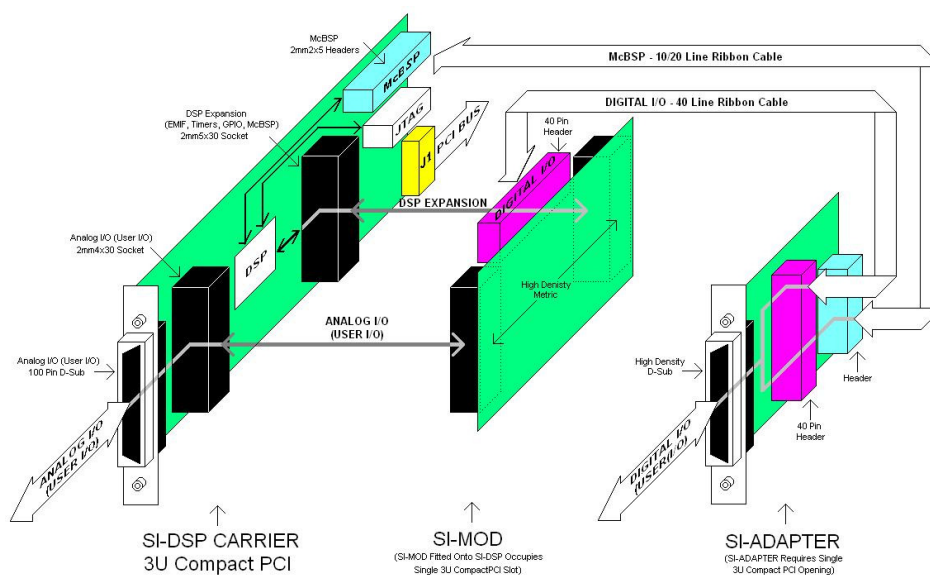
Memory Options

The SI-C6xDSP-cPCI is configured with conventional 144 pin SO-DIMM socket to accommodate standard, 3.3V non-buffered PC133 SDRAM modules used in laptops. The SI-C6xDSP-cPCI supports *half* of the capacity on 64MB, 128MB, 256MB, and 512MB module sizes, making it a very cost effective solution for the most demanding and memory intensive applications.

Hardware Support

The SI-C6xDSP-cPCI includes expansion connectors allowing for custom designs, or for attaching 'off the shelf' multifunction I/O modules from Sheldon Instruments. Sheldon Instruments offers several daughter modules for multichannel analog and digital I/O, including 4 to 64 channels of 16 bit ADCs and DACs.

Expandability Diagram





Software Support

The SI-C6xDSP-cPCI is available with extensive development tools from Sheldon Instruments and TI.

For quick turnkey development, Sheldon Instruments offers [QuVIEW](#) and [QuBASE](#), which are a set of DSP-resident libraries for real time performance that greatly accelerate data acquisition, signal processing, and control applications. [QuVIEW](#) is a real time accelerator for LabVIEW, and [QuBASE](#) a real time accelerator for Visual Basic. A full range of examples and tutors are provided to demonstrate their ease of use and breadth of functionality and capabilities. [QuBASE](#) runs under Windows, while [QuVIEW](#) also runs under Linux.

When purchased as a DSP evaluation board, Sheldon Instruments also includes sample DSP and Windows and Linux 32/64 bit device driver source code to accompany TI's development environment. The DSP source code illustrates full communication modes, and the Windows or Linux 32/64 bit device driver source code includes the complete **SI-DDK**, along with COFF file loader utilities.



Technical Specifications

Processor for SI-C671xDSP-cPCI:

- 225-300Mhz TMS320C6713.
- 16 DSP DMA channels, 2 cPCI/PXI DMA channels.

Memory:

- SDRAM program and data memory:
 - Standard 3.3V, non-buffered PC133 SDRAM in SODIMM format.
 - Sizes: 64MB, 128MB, 256MB and 512MB, with x16 organizations. Only half of capacity is used.
 - PC133 SDRAM module clocked from E Clock running at 75Mhz, maximum delay of memory ICs mounted on module not to exceed 7.5 nsec.
 - Single bank SO-DIMMs: supports *half* of memory ICs mounted on single bank modules, with all capacity only mapped on CE2 (DSP memory region starting at 0xA0000000). The DSP's CE3 region is left empty (DSP memory region starting at 0xB0000000).
 - Dual bank SO-DIMMs: supports *half* of memory ICs mounted on dual bank modules, with quarter of module capacity mapped on CE2 (DSP memory region starting at 0xA0000000), and the second quarter mapped on CE3 (DSP memory region starting at 0xB0000000).
 - Host accessible while DSP is active, with multiple communication options.
- Boot memory:
 - 512kx8 SRAM or 2Mx8 Flash memory.
 - Configured as Dual Access memory: Accessible by host (only while DSP is inactive/reset) for downloading COFF files. Accessed by DSP during its boot loading process.
 - Mapped on CE1 (DSP memory region starting at 0x90000000).

Interface to Host:

- cPCI/PXI initiated bus master transfer speeds:
 - Up to 132Mbyte/sec bursts with block sizes of eight (8) 32 bit words.
 - Up to 25Mbyte/sec sustained transfers of any block size, using DMA.
- Eight 32 bit, bi-directional communications modes between TMS320C6x and the PCI9054:
 - Host target/slave access mode, combined with DSP I/O or DSP's DMA engine.
 - Block Mode DMA Bus Master mode, using the PCI9054 as the cPCI/PXI bus master, combined with DSP I/O or DSP's DMA engine.
 - cPCI/PXI Initiated/Local Master with the DSP as the cPCI/PXI bus master, with DSP I/O or DSP's DMA engine.
- The PCI9054's internal registers are tied onto the C6x's EMIF bus, mapped on CE0 (DSP memory region starting at 0x80000000).
- Four C6x routable interrupts:
 - Up to three C6x interrupts can be routed for basic communication and DMA synchronization.
 - Up to two C6x interrupts can be routed to expansion connectors.



Peripheral Expansion:

- Two 2mm socket connectors, and one external 100 pin half pitch DSUB connector:
 - DSP Expansion: First external 2mm pitch, 5x30 (150 contacts) socket connector for interfacing the expansion board to the DSP's bus, or linking to all of the DSP's peripheral ports (McBSP, McASP, HPI/GPIO, Timers).
 - User I/O: Second external 2mm pitch, 4x30 (120 contacts) socket connector for interfacing external user defined signals to custom daughter board. Linked only to externally accessible 100 pin half pitch DSUB connector.
 - External 100 pin, half pitch (0.050"), Series III DSUB connector for interfacing external user defined signals to the 2mm User I/O connector. AMP part 787169-9, 787170-9, or 787362-9.
- DSP Expansion 2mm connector decodes 64Kx32 words, mapped into the DSP's EMIF bus, which contains the following signals:
 - Address: A15-A0 (DWord Boundary).
 - Data: D31-D0.
 - Control: X_R/Wn, X_CS_n, X_INT[1:0] (software routable to DSP's EXTINT[7:4]), X_RDY, X_CLK[1:0].
 - Peripheral Port: McBSP[1:0], HPI/GPIO, TINP[1:0], TOUT[1:0].
 - Host +3.3Vdc, +5Vdc, +/-12Vdc, +1.8Vdc & GND.
- Two 2mm pitch, 2x5 (10 contacts) headers: McBSP0 and McBSP1.
- One 14 pin header for JTAG port.

Software:

- Windows and Linux 32/64 bit driver support.
- Extensive [QuVIEW](#) DSP-resident libraries for LabVIEW, including examples for real time acquisition, signal processing, and control.
- Extensive [QuBASE](#) DSP-resident libraries for Visual Basic, including examples for real time acquisition, control and analysis.
- Sample code for COFF loaders, PC <-> DSP communications source code and SI-DDK.
- Compatible with separately purchased TI debuggers, C/C++ compilers, assemblers and linkers.

Physical Dimensions, Electrical Requirements, Temperature:

- 3U size cPCI/PXI bus card measuring 160mm(L) x 100mm(H).
- 0.31lbs or 140 grams.
- Supply Voltages: 3.3V for all circuitry, and 5V for expansion bus buffers; 3V expansion buffers may be placed on special request. +/-12V supplies passed on to expansion connector.
- 4.5 watts (3.3V @ 1.5A) typical with 128MB SDRAM.
- Commercial grade 0-85C. Consult factory for availability of industrial and military temperature grades.

Ordering Information:

- SI-C6713DSP-cPCI:
 - SI-C6713DSP-cPCI-64.
 - SI-C6713DSP-cPCI-128.
 - SI-C6713DSP-cPCI-256.



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