

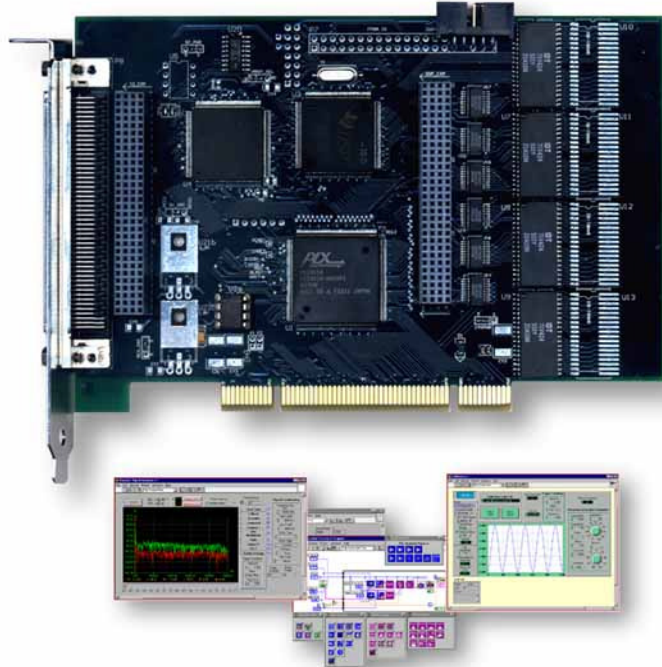


SI-C33DSP-PCI

TMS320VC33 DSP Board for PCI Bus

Key Features

- 150 MFLOPS peak performance, 32 bit floating point precision.
- 128Kx32 words of one (1) wait state Dual Access SRAM Memory, expandable to 1Mx32 words.
- Full bi-directional PCI initiated bus mastering, with 132MB/sec peak transfer rate.
- Memory mapped host communications port.
- Software development tools from Sheldon Instruments includes **QuVIEW**, **QuBASE** and the **SI-DDKs**; as well compatibility with separately purchased TI and third party tools.
- Windows and Linux 32/64 bit drivers and sample application support.
- Expansion connectors for prototyping, analog & digital I/O daughter cards.
- JTAG port for in system development and debugging.



Introduction

The SI-C33DSP-PCI from Sheldon Instruments is a powerful Digital Signal Processor (DSP) card for your PC equipped with a PCI bus. It is based on Texas Instruments' new 150Mhz TMS320VC33, 32 bit floating point DSP, and can transform your PC into an ultra high performance development system and DSP accelerator. A full line of software development tools are available from Sheldon Instruments and TI, which include compilers, assemblers, linkers, and debuggers.



Host PCI bus to DSP Link

All communication between the host and the DSP take place by means of PLX's PCI 9054 IC. Three (3) methods may be used for data transfer between the PCI bus and the DSP's memory: dual access mode, PCI initiated bus mastered transfer mode with the 9054 acting as the bus master, and bus mastering with the DSP acting as the PCI bus master.

For the dual access mode, all of the DSP's zero wait state SRAM memory is simultaneously accessible by both the PCI bus and the DSP with the 9054 behaving as a target peripheral. The DSP's memory is directly mapped into the first target region of the 9054, which can be accessed with standard memory access calls.

Onboard control logic arbitrates the appropriate timing between the C33's primary bus, the SRAM, and the 9054's Local bus. This is accomplished by asserting the C33 HOLD signal for no more than three (3) of its own clock cycles, every time the PCI side performs an access.

In addition to the dual access memory, large blocks of data can be transferred using PCI bus master transfers. The first bus master transfer method involves using the 9054's DMA capabilities to access the DSP memory. The second bus master transfer method allows the DSP to act as the PCI bus master, where it actually has direct access to the host computer's main memory! Both PCI bus master methods may allow for the highest possible burst transfer rates to take place over the PCI bus without host processor intervention.

Hardware Support

The SI-C33DSP-PCI includes expansion connectors allowing for custom designs, or for attaching 'off the shelf' multifunction I/O modules from Sheldon Instruments. Sheldon Instruments offers several daughter modules for multichannel analog and digital I/O, including 4 to 64 channels of 16 bit ADCs and DACs.

Software Support

The SI-C33DSP-PCI is available with extensive development tools from Sheldon Instruments and TI.

For quick turnkey development, Sheldon Instruments offers [QuVIEW](#) and [QuBASE](#), which are a set of DSP-resident libraries for real time performance that greatly accelerate data acquisition, signal processing, and control applications. [QuVIEW](#) is a real time accelerator for LabVIEW, and [QuBASE](#) a real time accelerator for Visual Basic. A full range of examples and tutors are provided to demonstrate their ease of use and breadth of functionality and capabilities. [QuBASE](#) runs under Windows, while [QuVIEW](#) also runs under Linux.

Typical benchmarks for a 150Mhz C33 processor include the computation of a 1024 point Radix-2 complex FFT at 400us.

When purchased as a DSP evaluation board, Sheldon Instruments also includes free sample DSP and Windows or Linux 32/64 bit device driver source code to accompany TI's development environment. The DSP source code illustrates full communication modes, and the Windows or Linux 32/64 bit device driver source code includes the complete **SI-DDK**, along with COFF file loader utilities.



Technical Specifications

Processor for SI-C33DSP-PCI:

- TMS320VC33 150Mhz DSP.
- Dual DMA channel.

Memory Options:

- "-128" option:
 - 128K x 32 bit words one (1) wait state dual access SRAM on C33's primary bus.
- "-512" option:
 - 512K x 32 bit words one (1) wait state dual access SRAM on C33's primary bus.
- "-1M" option:
 - 1M x 32 bit words one (1) wait state dual access SRAM on C33's primary bus.

Interface to Host:

- PCI initiated bus master transfer speeds:
 - Up to 132Mbyte/sec bursts with block sizes of eight (8) 32 bit words.
 - Up to 12Mbyte/sec sustained transfers of any block size, using DMA.
- Four 32 bit, bi-directional communications modes between TMS320C33 primary bus and the 9054:
 - Target/Dual access mode.
 - Block Mode DMA Bus Master mode, using the 9054 as the PCI bus master.
 - PCI Initiated/Local Master with DSP I/O, using the DSP as the PCI bus master.
 - PCI Initiated/Local Master with DSP DMA, using the DSP's DMA as the PCI bus master.
- The 9054's internal registers are mapped into the C33's primary bus, address space starting at 0xFF0000.

- INTO used by C33 for basic communication and DMA transfer initialization; INT2 and INT3 available on DIN expansion connectors.

Peripheral Expansion:

- Two 2mm socket connectors, and one external 100 pin half pitch DSUB connector:
 - DSP Expansion: First external 2mm pitch, 4x30 (120 contacts) socket connector for interfacing the expansion board to the DSP's bus. Nominal 4.3V CMOS/TTL logic levels, directly tied to 74FCT2245 class of bidirectional buffers.
 - User I/O: Second external 2mm pitch, 4x30 (120 contacts) socket connector for interfacing external user defined signals to custom daughter board. Linked only to externally accessible 100 pin half pitch DSUB connector.
 - External 100 pin, half pitch (0.050"), Series III DSUB connector, designated P8, for interfacing external user defined signals to P6. AMP part 787169-9, 787170-9, or 787362-9.
- P5 120 pin metric connector decodes 8Kx32 words, mapped into the DSP's primary bus, address space ranging from 0xFE0000 to 0xFE1FFF.
- DSP Expansion 2mm connector decodes 64Kx32 words, mapped into the DSP's EMIF bus, which contains the following signals:
 - Address: A[15:0] (DWord Boundary).
 - Data: D[31:0].
 - Control: R/W, STRB, XINT[0:1] (DSPINT[2:3]), RDY, XCLK[0:1] (DSP H[1:3]).
 - Host +3.3Vdc, +5Vdc, +12Vdc, -12Vdc, regulated +1.8Vdc, and GND.
- One 16 pin header for DSP I/O signals: Serial port 0, XF[0:1], TMCK[0:1].
- One 14 pin header for JTAG port.

**Software:**

- Windows and Linux 32/64 bit driver support.
- Extensive QuVIEW DSP-resident libraries for LabVIEW, including examples for real time acquisition, signal processing, and control.
- Extensive QuBASE DSP-resident libraries for Visual Basic, including examples for real time acquisition, signal processing, and control.
- Sample code for COFF loaders, PC <-> DSP communications source code and SI-DDK.
- Compatible with separately purchased TI debuggers, C/C++ compilers, assemblers and linkers.

Physical Dimensions, Electrical Requirements, & Temperature:

- Half size PCI-bus card measuring 6.4"(L) x 3.9"(H).

- 0.31lbs or 140 grams.
- Supply Voltages: 3.3V for all circuitry, and 5V for expansion bus buffers; 3V expansion buffers may be placed on special request. +/-12V supplies passed on to expansion connector and not used by onboard circuitry.
- 1.5 watts typical (3.3V @ 0.5A) with 128Kx32 words SRAM.
- Commercial grade 0-85C. Consult factory for availability of industrial and military temperature grades.

Ordering Information:

- SI-C33DSP-PCI:
 - SI-C33DSP-PCI-128.
 - SI-C33DSP-PCI-512.
 - SI-C33DSP-PCI-1M.

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